

Date	Revision	Item
February 07 2005	Ver1.0	First released
April 21 2005	Ver 1.1	Add support SDA physical layer 1 Ver 1.1
July 01 2005	Ver1.2	Add 256MByte model

MicroSD Card Specification

Model Name :

KT032S4CCS

KT032S4CMH

KT064S4DAS

KT064S4DBS

KT064S4DMH

KT128S4EMH

KT128S4EAS

KT256S4EAS

Ver 1.2

07.01.2005

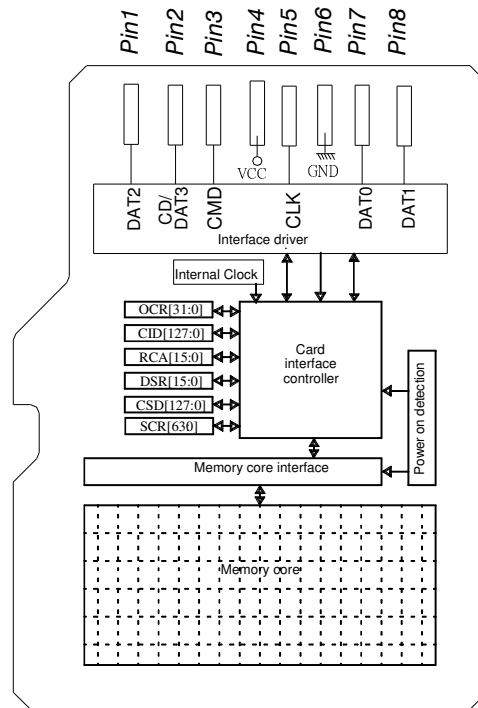
Features

- Capacity:32MB/64MB/128MB
- Compliant SD Card Specification Ver 1.01
- Physical Layer specification Part 1 Ver 1.1 (Function, Electrical Characteristic, Registers)
- Compliant MicroSD Specification Ver 1.0
- On card error correction
- Two alternative communication protocols: SD mode and SPI mode
- Variable clock rate 0~25MHz.
- Variable clock rate 0~50MHz. For SDA Ver1.1.
- Voltage operating :2.7~3.6V.
- Low power consumption : automatic power down and automatic wake up, smart power management
- No external programming voltage required.
- Damage free powered card insertion and removal
- Support CPRM
- Password protection of cards.
- High speed serial interface with random access a cost-effective solution with ultra high performance of flash access time and high reliability of data storage.
- Up to 10 stacked card(at 20MHZ,VCC=2.7~3.6V)
- Data Endurance: 100k Program/Erase Cycles
- Easy handling for the end user
- Reliable electrical interconnection
- Bearing textual information and image
- PIP package Technology
- Dimension: 11mm(W)x15mm(L)
- Thickness: inter connect area:0.7mm
Card thickness:0.95mm
- Add MicoSDcard adapter can be use in SD card socket.

Description

These MicroSD cards are highly integrated flash memories with serial and random access capability. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission. This interface allows several cards to be stacked by through connecting their peripheral contacts. MicroSD cards are fully compatible to a new consumer standard, called the MicroSD card system standard define in the SD card and MicroSD card System specification. The system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. MicroSD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors mobile, battery-powered application such as audio players, organizers, palmtops, electronic books, encyclopedia and dictionaries. Using very effective data compression schemes such as MPEG, the MicroSD card will deliver enough capacity for all kinds of multimedia data.

Block Diagram



All units these MicroSD card are clocked by an internal clock generator. The interface driver unit synchronizes the DAT and CMD signals from external CLK to the internal used clock signal. The card is controlled by the six line MicroSD card interface containing the signals: CMD,CLK,DAT0~DAT3. For the identification of the MicroSD card in stack , a card identification register(CID) and a relative and address register (RCA) is foreseen. An additional register contain different types of operation parameter. This register is called (CSD). The communication using the MicroSD card lines to access either the memory field or the register is defined by the SD card standard. The card has its own power on detected unit. No additional master reset signal is required to setup the card after power on. It is protected against short circuit during insertion and removal while the MicroSD card system is power up. No external programming Voltage supply is required. The programming voltage is generated on card. These MicroSD card support a second interface operation mode the SPI interface mode. The SPI mode is active if the CS signal is asserted(negative) during the reception of the reset command(CMD0).

Interface

These MicroSD Card interface can operate in two different modes:(please refer to SD card specification, part1, physical layer, version 1.01).

- . SD Card mode
- . SPI mode

Host system can choose either one of modes. SD Card mode allow the 4-bit high performance data transfer. SPI mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss performance, relatively to the SD mode.

MicroSD Card mode pin definition

Pin	Name	Type ¹	Description
1	DAT2	I/O/PP	Data bit 2
2	CD DAT3 ²	I/O/PP ³	Card Detect Data bit 3
3	CMD	PP	Command/Response
4	V _{CC}	S	Supply Voltage
5	CLK	I	Clock
6	V _{SS}	S	Ground
7	DAT0	I/O/PP	Data bit 0
8	DAT1	I/O/PP	Data bit 1

- 1: S: Power Supply, I: Input O: Output I/O: Bi-directionally PP: I/O using push-pull drivers.
2. The extended DAT lines(DAT1-DAT3) are input on power on. They start to operate as DAT lines after SET_BUS-WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode ,as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.
3. After power on this line is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

SD Card Bus Concept

The SD bus allows the dynamic configuration of the number of data lines from 1 to 4 Bi-directional data signal. After power up by default, the MicroSD card will use only DAT0. After initialization, host can change the bus width. Multiplied MicroSD cards connections are available to the host. Common V_{CC}, V_{SS}, and CLK signal connections are available in the multiple connection. However, Command, Respond and Data line(DAT0~DAT3) shall be divided for each card from host.

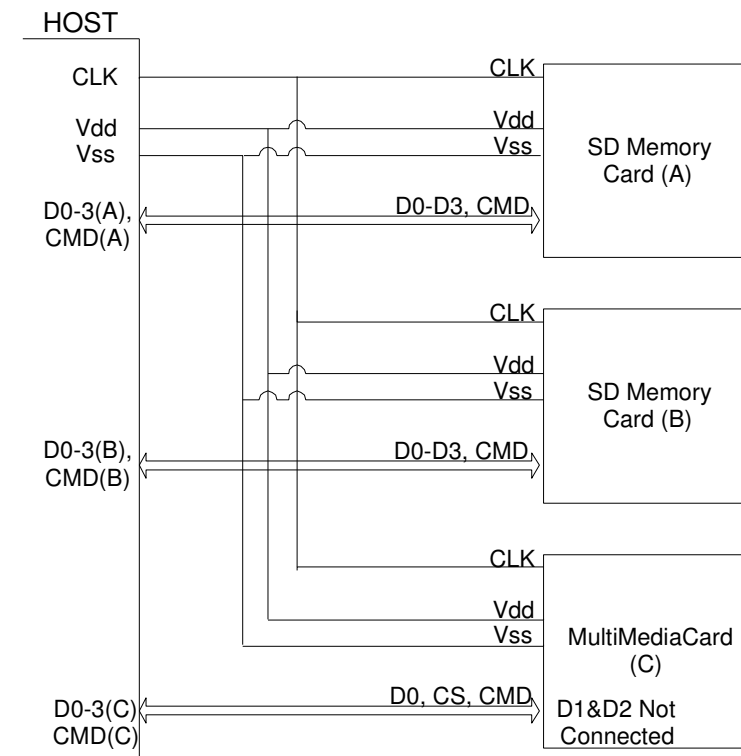
This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit terminated by stop bit.

CLK: with each cycle of this signal a one bit transfer on the command and data lines are done. The frequency may vary between zero and the maximum clock frequency. The MicroSD Card bus master is free to generate these cycles without restriction in the range of 0 to 25Mhz(low speed), 0 to 50Mhz(high speed).

CMD: Commands are transfer serially on the CMD line. A command is a token to starts an operation from host to the card. Commands sent to a address single card(address command) or to all connected cards(boardcast command).

Responses are transfer serially on the CMD line. A response is a token to answer to a previous command. Responses are sent from a single card or from all connected cards.

DAT0~3: Data can be transfer from the card to host or vice versa. Data is transferred via the data line.



SD Card bus Topology

SPI mode pin definition

Pin	Name	Type ¹	Description
1	RSV	-	
2	CS	I	Chip Select(Neg. True)
3	DI	I	Data In
4	V _{CC}	S	Supply Voltage
5	CLK	I	Clock
6	V _{SS}	S	Ground
7	DO	O/pp	Data Out
8	RSV	-	

1 S: Power Supply, I: Input O: Output I/O: Bi-directionally PP: I/O using push-pull drivers

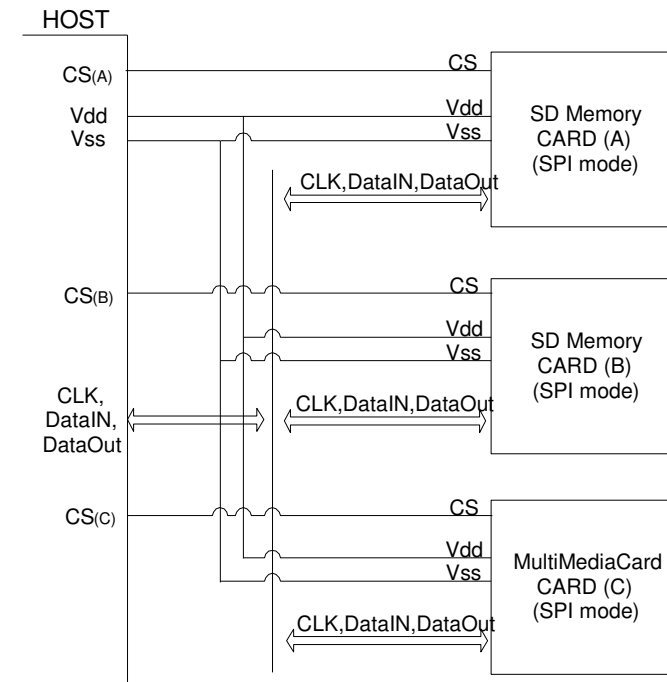
Note: These signals should be pulled up by host side with 10~100K ohm resistance in the SPI mode.

SPI Bus Concept

The SPI bus allows one bit data line by 2-channel(Data In and Out). The SPI compatible mode allows the MMC Host systems to use MicroSD card with little change. SPI mode is byte transfers.

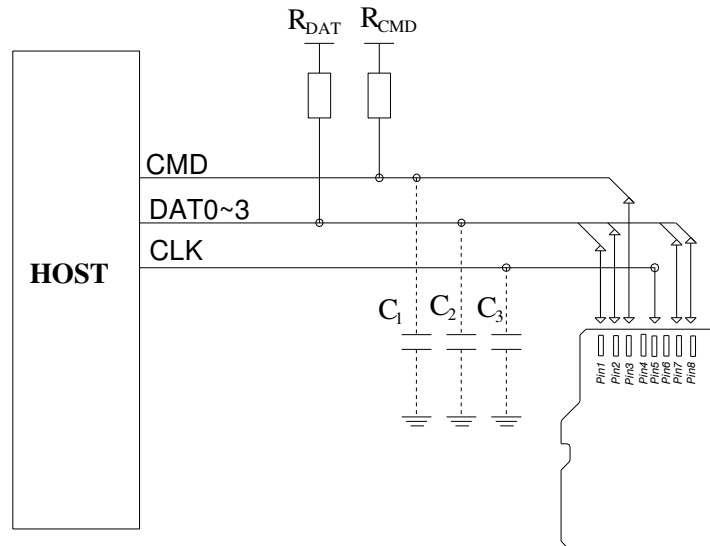
All the data token are multiples of the bytes(8 bit) and always byte aligned to the CS signal. The advantage of the SPI mode is reducing the host design in effort. Especially, MMC host can be modified with little change.

The disadvantage of the SPI mode is the loss of performance versus SD card mode.



SPI mode bus topology

MicroSD Card Electrical Characteristics



T-Flash card Connection diagram

Bus Operation conditions

General

Parameter	Symbol	Min	Max.	Unit	Remark
Peak Voltage on all line		-0.3	V _{CC} +0.3	V	
Input Leakage Current		-10	10	uA	
Output Leakage Current		-10	10	uA	

Power Supply Voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply Voltage	V _{CC}	2.7	3.6	V	
Supply Voltage (VSS ₁ , VSS ₂)		-0.3	0.3	V	
Power up Time			259	ms	From 0V to V _{CC} Min.

The current consumption of any card during the power-up period until the first command occur must not exceed 15mA averaged over 1 second. From first command until 'stby_state'(the state that the host may read CSD and verify the operating current consumptions) the maximum current consumption may be 100mA averaged over 1 second. Note that a card that is delivered before fixing physical Spec Ver 1.01 , mat not meet the above initialization current restrictions.

Bus Signal Line Load

The total capacitance C_L the CLK line of the SD memory card bus is the sum of the bus master capacitance C_{HOST} , the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line: $C_L = C_{HOST} + C_{BUS} + N * C_{CARD}$

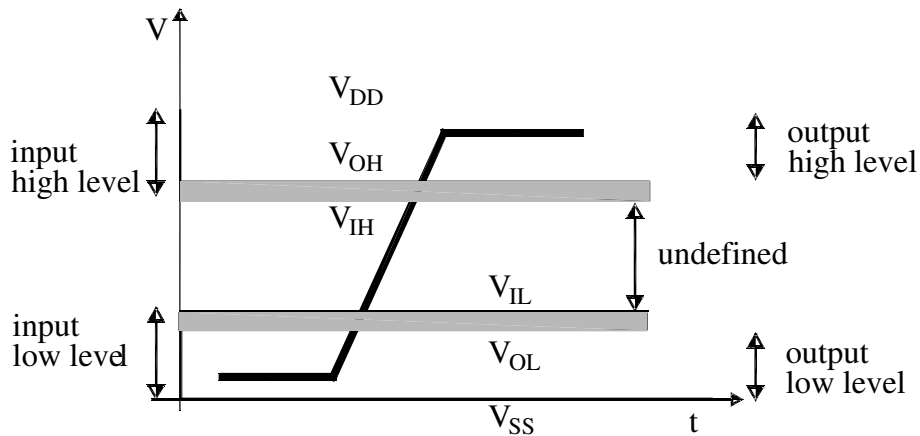
Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30pF for up to 10 cards, and 40 pF for up to 30cards, the following values must not be exceeded:

Parameter	Symbol	Min.	Max.	Unit	Note
Pull-up resistance for CMD	R_{CMD}	10	100	K Ω	Prevent bus floating
Pull-up resistance for DAT	R_{DAT}	10	100	K Ω	Prevent bus floating
Bus Signal Line Capacitance	C_L	-	250	pF	$F_{pp} < 5\text{MHz}, 21\text{cards}$
Bus Signal Line Capacitance	C_L	-	100	pF	$F_{pp} < 20\text{MHz}, 7\text{cards}$
Single Card Capacitance	C_{CARD}	-	10	pF	
Maximum Signal line Inductances		-	16	nH	$F_{pp} < 20\text{MHz}$
Pull-up resistance inside card(Pin1)	R_{DAT3}	10	90	K Ω	May be used for card detecion

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST} , C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Bus Signal Levels

As the bus can be supplied with variable supply voltage , all signal levels are related to the supply voltage.

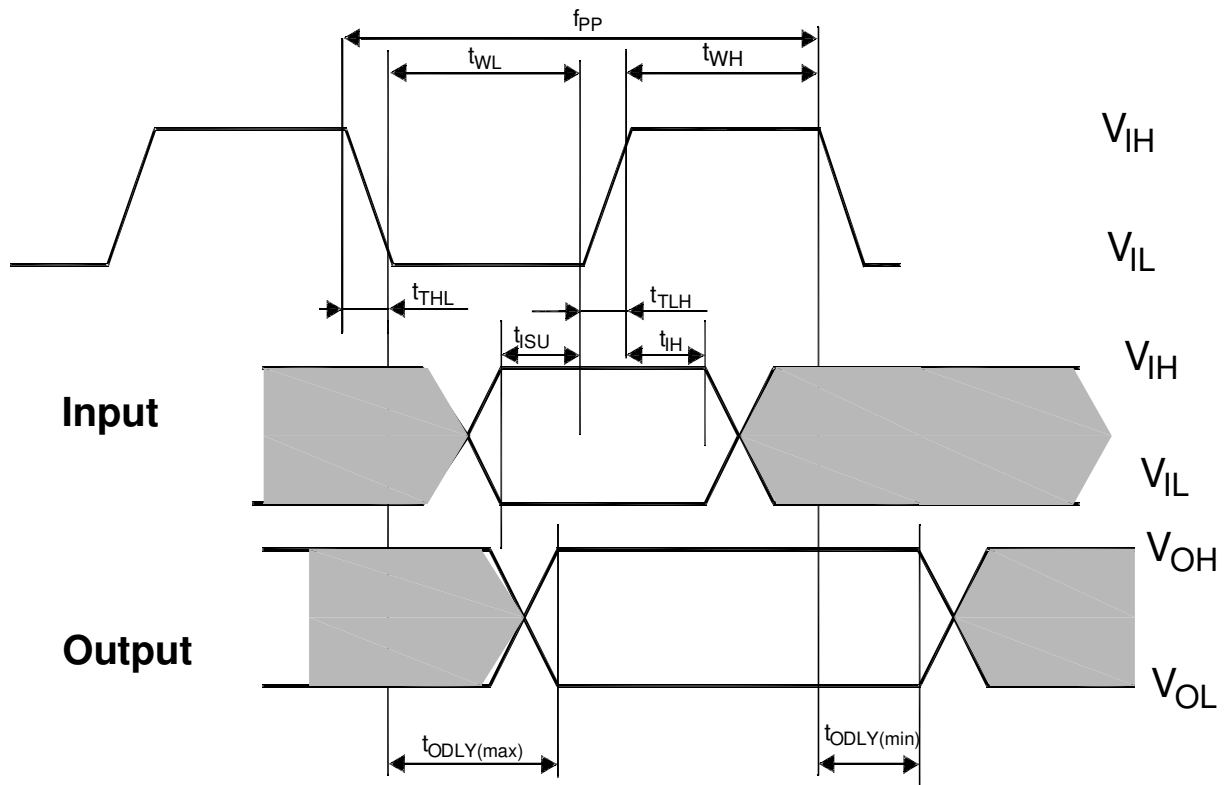


To meet the requirement of the JEDEC specification JESD8-1A, the card input and output voltage shall be within the following specified ranges for any V_{CC} of the allowed voltage range

Parameter	Symbol	Min	Max.	Unit	Remark
Output High Voltage	V_{OH}	$0.75 \times V_{CC}$		V	$I_{OH} = -100\mu\text{A} @ V_{CC} \text{ min}$
Output Low Voltage	V_{OL}		$0.125 \times V_{CC}$	V	$I_{OL} = -100\mu\text{A} @ V_{CC} \text{ min}$
Input High Voltage	V_{IH}	$0.625 \times V_{CC}$	$V_{DD} + 0.3$	V	
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.25 \times V_{CC}$	V	

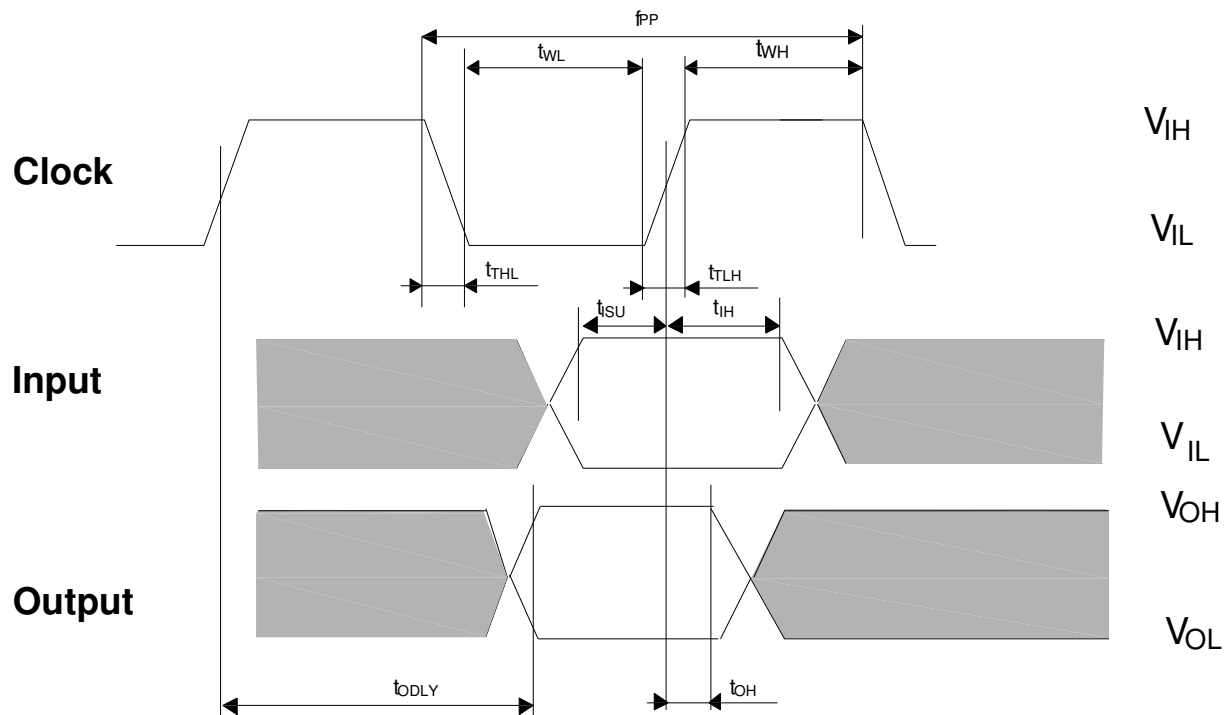
Bus Timing(low-speed mode)

Parameter	Symbol	Min.	Max.	Unit	Note
Clock Frequency Data Transfer Mode	F _{PP}	0	25	MHz	C _L ≤100pF(7Cards)
Clock Frequency identification Mode	F _{OD}	0	400	KHz	C _L ≤250pF(21Cards)
Clock Low time	t _{WL}	10		ns	C _L ≤100pF(7Cards)
Clock High time	t _{WH}	10		ns	C _L ≤100pF(7Cards)
Clock Rise time	T _{TLH}		10	ns	C _L ≤100pF(7Cards)
Clock Fall time	T _{THL}		10	ns	C _L ≤100pF(7Cards)
Clock Low time	t _{WL}	50		ns	C _L ≤250pF(21Cards)
Clock High time	t _{WH}	50		ns	C _L ≤250pF(21Cards)
Clock Rise time	T _{TLH}		50	ns	C _L ≤250pF(21Cards)
Clock Fall time	T _{THL}		50	ns	C _L ≤250pF(21Cards)
Input Set-up Time	T _{ISU}	5		ns	CMD,DAT Reference to CLK
Input Hold Time	T _{IH}	5		ns	CMD,DAT Reference to CLK
Output Delay Time during Data Transfer Mode	T _{ODLY}	0	14	ns	CMD,DAT Reference to CLK
Output Delay Time during identification Mode	T _{ODLY}	0	50	ns	CMD,DAT Reference to CLK



Bus Timing(high-speed Mode)

Parameter	Symbol	Min.	Max.	Unit	Note
Clock Frequency Data Transfer Mode	F _{PP}	0	50	MHz	
Clock Low time	t _{wL}	7		ns	
Clock High time	t _{wH}	7		ns	
Clock Rise time	T _{TLH}		3	ns	
Clock Fall time	T _{THL}		3	ns	
Input Set-up Time	T _{ISU}	6		ns	
Input Hold Time	T _{IH}	2		ns	
Output Hold time	T _{OH}	2.5		ns	
Output Delay time during Data Transfer Mode	T _{ODLY}		14	ns	



System Environment Specification

ESD (contact Pads)		-4	4	KV	
Operation Temperature	T _{OTG}	-25	85	°C	
Operation Humidity	25°C, 95%				
Storage Temperature	T _{STG}	-40	85	°C	
Storage Humidity	40°C, 93%				

Card Register
OCR Register

OCR Bit Position	VDD Voltage Window	Capacity			
		32MB	64MB	128MB	256MB
31	Card power up status Bit(busy)	0=busy 1=ready			
30~24	reserved	0			
23	3.6~3.5	1			
22	3.5~3.4	1			
21	3.4~3.3	1			
20	3.3~3.2	1			
19	3.2~3.1	1			
18	3.1~3.0	1			
17	3.0~2.9	1			
16	2.9~2.8	1			
15	2.8~2.7	1			
14	2.7~2.6	0			
13	2.6~2.5	0			
12	2.5~2.4	0			
11	2.4~2.3	0			
10	2.3~2.2	0			
9	2.2~2.1	0			
8	2.1~2.0	0			
7	2.0~1.9	0			
6	1.9~1.8	0			
5	1.8~1.7	0			
4	1.7~1.6	0			
3~0	reserved	0			

CID Register

Field	Width	CID-slice	Capacity			
			32MB	64MB	128MB	256MB
MID	8	[127:120]	13 h			
OID	16	[119:104]	4b47 h			
PNM	40	[103:64]	SD032	SD064	SD128	SD256
PRV	8	[63:56]	10 h			
PSN	32	[55:24]	Product serial Number			
-	4	[23:20]	0 h			
MDT	12	[19:8]	Manufacture date			
CRC	7	[7:1]	CRC			
-	1	[0:0]	1h			

CSD Register

Field	Width	Cell Type	CSD slice	Value			
				32MB	64MB	128MB	256MB
CSD_Structure	2	R	[127:126]	00			
-	6	R	[125:120]	000000			
TAAC	8	R	[119:112]	01011110			
NSAC	8	R	[111:104]	00000000			
TRAN_SPEED	8	R	[103:96]	00110010			
CCC	12	R	[95:84]	000111110101			
READ_BL_LEN	4	R	[83:80]	1001			
READ_BL_PARTIAL	1	R	[79:79]	1			
WRITE_BLK_MISALIGN	1	R	[78:78]	0			
READ_BLK_MISALIGN	1	R	[77:77]	0			
DSR_IMP	1	R	[76:76]	0			
-	2	R	[75:74]	00			
C_SIZE	12	R	[73:62]	E97 h	EF7 h	F27 h	F3F h
VDD_R_CURR_MIN	3	R	[61:59]	101			
VDD_R_CURR_MAX	3	R	[58:56]	101			
VDD_W_CURR_MIN	3	R	[55:53]	101			
VDD_W_CURR_MAX	3	R	[52:50]	101			
C_SIZE_MULT	3	R	[49:47]	010	011	100	101
ERASE_BLK_EN	1	R	[46:46]	0			
SECTOR_SIZE	7	R	[45:39]	1111111			
WP_GRP_SIZE	7	R	[38:32]	0000000	0000001	0000011	0000111
WP_GRP_ENABLE	1	R	[31:31]	1			
-	2	R	[30:29]	00			
R2W_FACTOR	3	R	[28:26]	101			
WRITE_BL_LEN	4	R	[25:22]	1001			
WRITE_BL_PARTIAL	1	R	[21:21]	0			
-	5	R	[20:16]	00000			
FILE_FOMAT_GRP	1	R/W(1)	[15:15]	0			
COPY	1	R/W(1)	[14:14]	0			
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0			
TMP_WRITE_PROTECT	1	R/W	[12:12]	0			
FILE_FORMAT	2	R/W(1)	[11:10]	00			
-	2	R/W	[9:8]	00			
CRC	7	R/W	[7:1]	(CRC)			
-	1	-	[0:0]	1			

SCR Register

Field	Width	CID-slice	Capacity			
			32MB	64MB	128MB	256MB
SCR_STRUCTURE	4	[63:60]	0			
SD_SPEC	4	[59:56]	1			
DATA_STAT_AFTER_ERASE	1	[55:55]	0			
SD_SECURITY	3	[54:52]	010			
SD_BUS_WIDTHS	4	[51:48]	0101			
-	16	[47:32]	0			
-	32	[31:0]	0			

Transfer Rate

Testing Condition

1. Main Board: MSI865PE Neo2
2. CPU: Intel Pentium 4 2.4GHz
3. DDR Memory: 256MByte
4. OS: Win2000 with SP4
5. Software: FD Bench Ver3.4
6. Testing Device: MicroSD card with adaptor and USB 2.0 Card Reader(GL819)

Capacity	Sequential Read	Sequential Write	Random Read	Random Write	Unit
32MB	10830	1759	9490	835	KB/s
64MB	10562	1970	9229	886	KB/s
128MB	10759	9510	10849	2212	KB/s
256MB	10849	10254	10552	1157	KB/s

Physical Outline Dimension

