xSil 248

(248-G)

Design Specification

for Embedded applications for Flash media

(CF, SM, xD, MS, MS PRO, MMC, SD, RS MMC, miniSD, MagicStor and Microdrive)

Rev. 0.90

2225 Martin Ave
Santa Clara, CA 95050.
www.onspecinc.com
sales@onspecinc.com
(408) 727 1819 x130

xSil 248 Design Specification
OnSpec Electronic, Inc.

REVISION HISTORY		
Date	Version	Reason for Change
May 6, 2005	0.90	Initial Datasheet

Document Title: General Specification for xSil 248.DOC

Format: Word for Windows

Date: May 8, 2005

Patents:
This product is covered by one or more of the following patents:
US Pat. 5841424, 6438638, 6832281, 6859361, 6859369
Taiwan Pat. I 222564
Other Foreign & US Patents Pending

Disclaimer:
Information in this document is provided in connection with OnSpec Electronic products. No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted by this document. Except as provided in OnSpec Electronic's Terms and Conditions of Sale for such products, OnSpec Electornic assumes no liability whatsoever, and OnSpec Electronic disclaims any express or implied warranty, relating to sale and/or use of OnSpec Electronic products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement or any patent, copyright or other intellectual property right.

OnSpec Electronic products are not intended for use in medical, life saving, or life sustaining applications.

Trademarks:
OnSpecLink Is a registered trademark of OnSpec Electronic, Inc.
All trademarks are the properties of their respective owners.

Table of Contents

TECHNICAL REFERENCE 5

1. INTRODUCTION 5

2. FUNCTION DESCRIPTION 6

2.1. PACKAGING 6
2.2. USB ENGINE 6
2.3. SERIAL EEPROM PORT 6
2.4. IDE/ ATAPI 6
2.5. SUPPORT FOR CF, MMC/ SD, MEMORY STICK, XD AND SMARTMEDIA CARDS 7
2.6. SERIAL PORT 7
2.7. GENERAL PURPOSE TIMERS 7
2.8. WATCHDOG TIMER 7
2.9. XSIL 248 PROCESSOR 7
2.10. RAM INTERFACE 7
2.11. MASKED ROM 7
2.12. PROGRAMMABLE READ AND WRITE CYCLES 8
2.12.1. PIN DESCRIPTION 8

3. ELECTRICAL CHARACTERISTICS 12

4.0 SMARTMEDIA TIMING 13

4.1 AC CHARACTERISTICS 13
4.2.1 READ CYCLE TIMING WAVEFORMS - 1MBYTE TO 32MBYTE 14
4.2.2 STATUS READ TIMING WAVEFORMS - 1MBYTE TO 32MBYTE 14
4.2.3. AUTOPAGE TIMING WAVEFORMS - 1MBYTE TO 32MBYTE 15
4.2.4 AUTO ERASE TIMING WAVEFORMS - 1MBYTE TO 32MBYTE 15
4.3.1 READ CYCLE TIMING WAVEFORMS - 64MBYTE TO 128MBYTE 16
4.3.2 STATUS READ TIMING WAVEFORMS - 64MBYTE TO 128MBYTE 16
4.3.3 AUTOPAGE TIMING WAVEFORMS - 64MBYTE TO 128MBYTE 17
4.3.4 AUTO ERASE TIMING WAVEFORMS - 64MBYTE TO 128MBYTE 17

5.0 XD PICTURE CARD TIMING DIAGRAMS 18

5.1 AC CHARACTERISTICS 18
5.2 READ CYCLE TIMING WAVEFORMS 19
5.3 STATUS READ TIMING WAVEFORMS 19
5.4 AUTOPAGE TIMING WAVEFORMS 20
5.5 AUTO ERASE TIMING WAVEFORMS 20

6. COMPACTFLASH TIMING 21

7. SECURE DIGITAL TIMING 22

8. MULTIMEDIACARD TIMING 23

9.MEMORY STICK TIMING 24

10. MEMORY STICK PRO TIMING 25

11. MMC 4.0 HOST OPERATION 26

11.1 FEATURES 26
11.2 MMC COMMUNICATION SIGNALS 26
11.2.1 MMC Card CLK Command 26
11.2.2 MMC Card CMD Command 26
11.2.3 MMC Card DAT0-DAT7 26
11.2.4 MMC Card Classes 26
11.3 MMC CARD INTERFACE PIN CONNECTIONS 27
11.4 MMC CARD REGISTERS 27
11.5 XSIL 248 MMC CARD HOST RESET 27
11.6 MMC CARD ARCHITECTURE 28
11.7 MMC FORM FACTOR 29
11.8 MMC BUS CONCEPT 29
11.9 MMC BUS LINES 29
11.10 MMC BUS PROTOCOL 30

12. PACKAGE DRAWING 32

12.1.1 100-pin package 32

13. PART NUMBER ORDERING INFORMATION 33

Tables and Figures

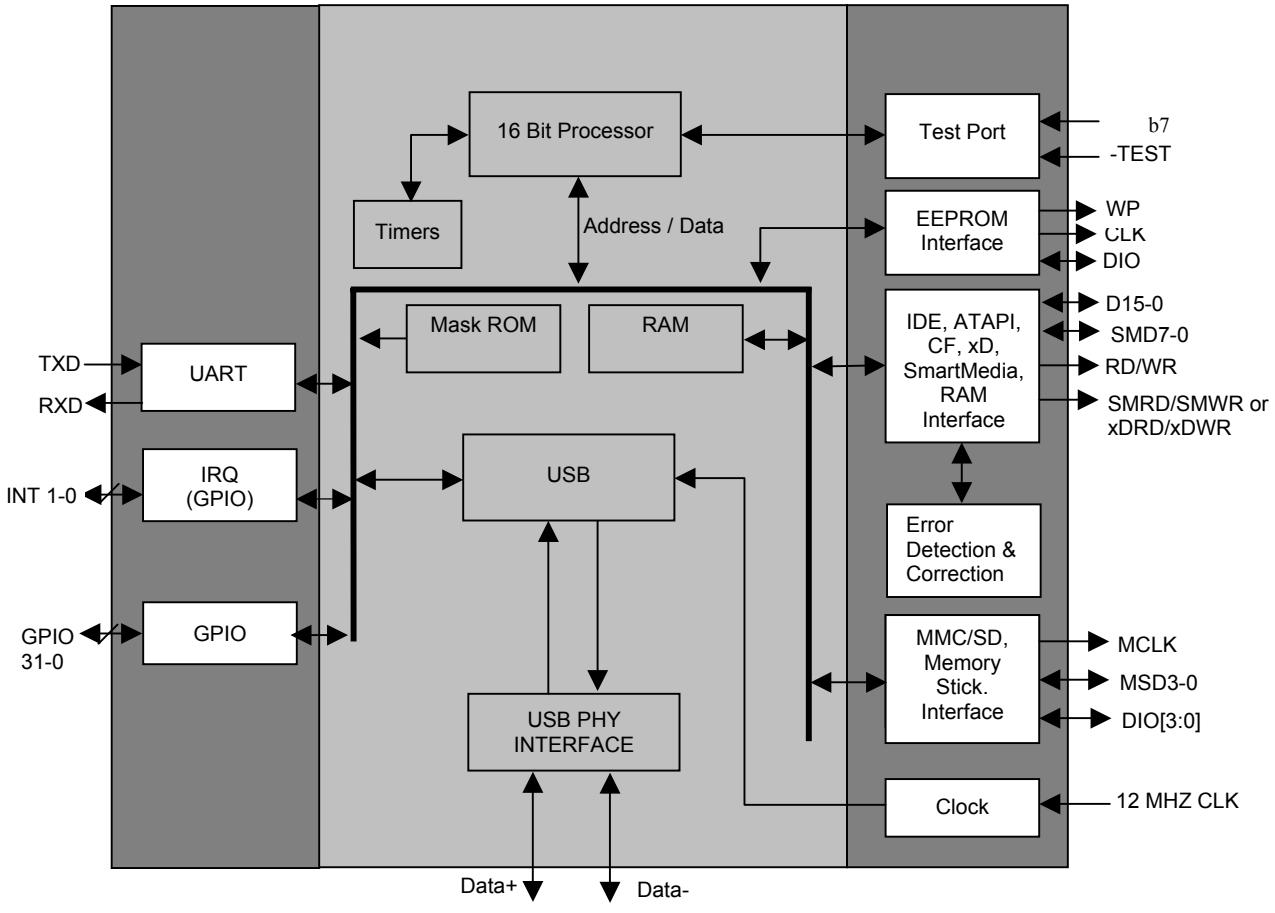
TABLE 1. XSIL 248 100 PIN DESCRIPTION 8
TABLE 1. XSIL 248 100 PIN DESCRIPTION (CONTD.) 9
TABLE 1. XSIL 248 100 PIN DESCRIPTION OPTION 1 (CONTD.) 10
TABLE 1. XSIL 248 100 PIN DESCRIPTION OPTION 1 (CONTD.) 11
TABLE 2. ELECTRICAL SPECIFICATIONS 12
TABLE 3. ABSOLUTE MAXIMUM RATINGS 12
TABLE 4. RECOMMENDED OPERATING CONDITIONS 12
TABLE 5. SMARTMEDIA AC CHARACTERISTICS 13
TABLE 6. XD PICTURE CARD AC CHARACTERISTICS 18
TABLE 7. PART NUMBER ORDERING INFORMATION 33

Technical Reference

- Universal Serial Bus Specification Version 2.0
- ATA-2 Specification for AT Attachment devices
- SFF 8020/8070 Specification for ATAPI devices
- SmartMedia™ Specification
- MMC™ Specification V2.11 or later
- SD™ Card Specification V1.0 or later
- xD™ Card Specification V1.0 or later
- Memory Stick™ Format Specification V1.40-00 or later (for MS Classic and HS™ devices)
- Memory Stick PRO™ Format Specification V1.00-01 or later

1. Introduction

The xSil 248 provides a low cost way to connect an IDE/ ATAPI/ Flash Memory Devices to USB 2.0 and USB 1.1 standards.



xSil 248 Block Diagram

2. Function Description

The xSil 248 is designed to connect an IDE/ATAPI device or Flash media to USB. It contains the following:

- 100-pin 16mm x 16mm QFP package
- Single chip with integrated USB 2.0 PHY
- Serial EEPROM port
- Supports up to 25 types of media. (Application notes available.)
- IDE/ ATAPI/ MMC™/ SD™/ Memory Stick™ / SmartMedia™/ xD™/ CF™ interface
- Support for High Speed operation of MMC/SD, Memory Stick and SmartMedia Cards
- Supports CompactFlash PIO Modes 0..6
- Supports SD Card High Speed mode (50MHz clock)
- Supports MMC media with 1-bit, 4-bit and 8-bit modes
- Support for MS PRO™, HS (4-bit mode)
- Supports SmartMedia ROM, Memory Stick ROM media
- Support for xD media, up to 2GB.
- Support for xD M series media – V1.2 xD Picture Card Specification compliant.
- Supports On-board NAND as a storage device, 8-bit and 16-bit
- 1-bit error correction and 2-bit error detection for SM and xD based on ECC.
- FEC Error detection and Correction, which can correct up to 2-bytes of error per sector with Parity data included.
- Firmware enhancements can be stored on On-board NAND when populated
- Serial port
- Two General Purpose Timers
- Watchdog Timer
- 16-bit Processor
- Programmable Read and Write widths
- Optimum hardware controlled transfer for speed and scalability

2.1. Packaging

The xSil 248 is a 100-pin QFP package.

2.2. USB Engine

The xSil 248 has a PIE interface, which meets the Universal Serial Bus (USB) specification V2.0 and V1.1. The PIE interface is capable of transmitting and receiving serial data at the USB High speed of 480 MegaBits/sec and Full speed of 12 MegaBits/sec. Internal High Speed PIE interface to USB 2.0 UTMI PHY.

2.3. Serial EEPROM Port

The xSil 248 provides a serial interface to access external EEPROM's. The interface is implemented using General Purpose I/O signals and can support a variety of serial EEPROM formats.

2.4. IDE/ ATAPI

The xSil 248 processor can be designed to interface to an IDE or ATAPI device. It supports PIO mode of data transfer.

2.5. Support for CF, MMC/ SD, Memory Stick, xD and SmartMedia Cards

The MultiMediaCard (MMC), Secure Digital Card (SD Card) and Memory Stick are serial access devices. They also require in-bound / out-bound data to be appended with CRC information. The xSil 248 processor provides support in hardware to generate the CRC and to convert Serial to Parallel and Parallel to Serial bit streams. A programmable clock speed is provided to set the clock speed based on the media's capabilities. The xSil 248 also provides Hardware ECC generation and checking for SmartMedia and XD. CF cards may be connected directly as an IDE device.

2.6. Serial port

Supports 7200 to 115.2K baud. Is useful as a debug port and can also be used to access the EEPROM for Reads / Writes from the serial port.

2.7. General Purpose Timers

Two general-purpose timers, Timer0 and Timer1 are provided to allow firmware programmers to keep track of timeouts as well as to generate delays.

2.8. Watchdog Timer

A Watchdog Timer is provided to enable catastrophic events to interrupt the processor. The Watchdog Timer overflow causes an internal processor reset. The Processor can read the WT bit after exiting reset to determine if the WT bit is set. If it is set, a watchdog timeout occurred. The timeout is selectable to any of the following values: 1 second, 4 seconds, 8 seconds or 16 seconds.

2.9. xSil 248 Processor

The xSil 248 Processor has a built-in 16-bit processor along with a BIOS ROM. The processor operates with a specialized instruction set optimized for Mass Storage applications and USB transaction processing. The start up code for the 16-bit processor resides in a masked ROM.

2.10. RAM Interface

The xSil 248 chip comes with an Internal RAM.

2.11. Masked ROM

The Masked ROM consists of the xSil 248 processor start-up code and the functions listed below:

- Power On Initialization
- USB packet transaction management
- USB Power Management (S0..S3 modes)
- USB Enumeration Management
- API support for USB transactions, EEPROM Interface, Memory Management etc.
- Built-in Library functions for IDE/ ATAPI and Flash devices

The firmware is easily extended / expanded by using External Serial EEPROM. The BIOS provides several services to facilitate this expansion code. At boot-up time, the scan services of the BIOS search for the expansion signature in the Serial EEPROM as well as via the UART and USB. For more information, refer to Applications section of this manual.

The BIOS API functions are designed as Software Interrupts, making it easy for enhancements. Any Interrupt can be enhanced / modified by inserting the user defined function in the interrupt placeholder.

When this interrupt is called by the BIOS, the user defined function is called first to enhance the behavior before passing it on to the standard BIOS function's call or return without passing it on.

2.12. Programmable Read and Write cycles

The external cycles to flash using the D[15:0], and SM[7:0] buss are software configurable.

2.12.1.Pin Description

The xSil 248 100 pin descriptions are shown below:

Table 1. xSil 248 100 Pin Description

Pin Number	Type	Signal	Drive (ma)	Function
1	In	X1		Oscillator
2	Out	X2		Oscillator
3	Power	AVdd		Analog 3.3V
4	Ground	AVss		Analog Ground
5	Analog	REF		Analog Reference
6	I/O	DM		USB DM
7	I/O	DP		USB DP
8	Power	AVdd		Analog 3.3V
9	Ground	AVss		Analog Ground
10	Ground	Vss		
11	Power	Vdd		2.5V
12	In	-TEST		Chip Test
13	Out	-SMRD	4	Smart Media, xD Read
14	Out	-SMWR	4	Smart Media, xD Write
15	Ground	Vss		
16	Power	Vdd		3.3V
17	I/O	SMD7	4	Smart Media, xD Data 7
18	I/O	SMD6	4	Smart Media, xD Data 6
19	I/O	SMD5	4	Smart Media, xD Data 5
20	In	-RESET		Power on Reset
21	I/O	SMD4	4	Smart Media, xD Data 4
22	I/O	SMD3	4	Smart Media, xD Data 3
23	I/O	SMD2	4	Smart Media, xD Data 2
24	I/O	SMD1	4	Smart Media, xD Data 1
25	I/O	SMD0	4	Smart Media, xD Data 0

Table 1. xSil 248 100 Pin Description (Contd.)

Pin Number	Type	Signal	Drive (ma)	Function
26	Ground	Vss		
27	Power	Vdd		3.3V
28	Out	-RD	4	CF, NAND Flash Read
29	Out	-WR	4	CF, NAND Flash Write
30	I/O	MSD3	4	Memory Stick Data 3
31	I/O	D15	4	CF, NAND Flash Data 15
32	I/O	MODE	4	
33	I/O	MSD2	4	Memory Stick Data 2
34	I/O	D14	4	CF, NAND Flash Data 14
35	I/O	MSD1	4	Memory Stick Data 1
36	I/O	D13	4	CF, NAND Flash Data 13
37	I/O	IO35	4	Memory Stick Clock
38	I/O	IO34	4	MMC Data 7
39	Power	Vdd		3.3V
40	I/O	D12	4	CF, NAND Flash Data 12
41	I/O	IO33	4	MMC Data 6
42	I/O	IO32	4	MMC Data 5
43	I/O	D11	4	CF, NAND Flash Data 11
44	I/O	IO29	4	LED
45	I/O	IO28	4	Memory Stick Power Control
46	I/O	D10	4	CF, NAND Flash Data 10
47	I/O	IO27	4	Memory Stick BS
48	Ground	Vss		
49	Power	Vdd		3.3V
50	I/O	IO26	4	LED

Table 1. xSil 248 100 Pin Description Option 1 (Contd.)

Pin Number	Type	Signal	Drive (ma)	Function
51	Ground	Vss		
52	Power	Vdd		3.3V
53	Power	Vdd		2.5V
54	In	RXD	4	Debug UART RXD
55	I/O	IO20	4	Memory Stick Data 0
56	Out	TXD	4	Debug UART TXD
57	I/O	IO25	4	LED
58	I/O	D9	4	CF, NAND Flash Data 9
59	I/O	IO19	4	MMC/SD Clock
60	I/O	D8	4	CF, NAND Flash Data 8
61	I/O	SDA	4	Serial EEPROM Data
62	I/O	D7	4	CF, NAND Flash Data 7
63	I/O	SCL	4	Serial EEPROM Clock
64	Power	Vdd		3.3V
65	I/O	D6	4	CF, NAND Flash Data 6
66	I/O	IO15	4	MMC/SD Data 3
67	I/O	D5	4	CF, NAND Flash Data 5
68	I/O	IO14	4	MMC/SD Data 2
69	I/O	D4	4	CF, NAND Flash Data 4
70	I/O	IO13	4	MMC/SD Data 1
71	I/O	D3	4	CF, NAND Flash Data 3
72	I/O	IO12	4	MMC/SD Data 0
73	I/O	D2	4	CF, NAND Flash Data 2
74	I/O	IO11	4	MMC/SD Power Control
75	Ground	Vss		

Table 1. xSil 248 100 Pin Description Option 1 (Contd.)

Pin Number	Type	Signal	Drive (ma)	Function
76	Power	Vdd	4	3.3V
77	I/O	D1	4	CF, NAND Flash Data 1
78	I/O	IO9	4	CF Power Control
79	I/O	D0	4	CF, NAND Flash Data 0
80	I/O	IO8	4	
81	I/O	IO31	4	NAND Flash 1 CS, MMC Data 4
82	I/O	IO7	4	MMC/SD MCMD
83	I/O	IO30	4	NAND Flash 1 Ready/Busy
84	I/O	WP	4	Serial EEPROM Write Protect
85	I/O	IO24	4	Smart Media, xD, NAND Flash CLE
86	I/O	IO5	4	CF CE2
87	I/O	IO23	4	Smart Media, xD, NAND Flash 0 CS
88	Ground	Vss		
89	Power	Vdd		3.3V
90	I/O	IO4	4	CF CE1
91	I/O	IO22	4	Smart Media, xD, NAND Flash ALE
92	I/O	IO3	4	CF Reset
93	I/O	IO21	4	Smart Media, xD, NAND Flash 0 Ready/Busy
94	I/O	IO2	4	CF Address 2
95	I/O	IO18	4	Smart Media, xD, NAND Flash Write Protect
96	I/O	IO1	4	CF Address 1
97	I/O	IO10	4	Smart Media, xD Power Control
98	Ground	Vss		
99	Power	Vdd		3.3V
100	I/O	IO0	4	CF Address 0

3. Electrical Characteristics

The various electrical, environmental and operating characteristics are provided below in tables 4-6.

Table 2. Electrical Specifications

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typical	Max		
V_{IH}	Input Voltage	2.0	-	-	V	
V_{IL}	(LVTTL,5V Tolerant)	-	-	0.8	V	
V_{IH}	Input Voltage	0.5×VDD	-	-	V	
V_{IL}	(3.3V PCI)	-	-	0.3×VDD	V	
V_{+}	Input Voltage	-	1.8	2.3	V	
V_{-}	(Schmitt)	0.5	0.9	-	V	
V_H		0.4	-	-	V	
V_{OH}	Output Voltage	2.4	-	-	V	IOH=-2mA to-24mA
V_{OL}		-	-	0.4	V	IOL= 2mA to 24mA
I_{IH}	Input Leakage Current	-10	-	10	µA	VIN= VDD
I_{IL}		-10	-	10	µA	VIN= GND
I_{OZ}	Output Leakage Current	-10	-	10	µA	Hi-Z state
I_{PU}	Pull-up Current	-22	-66	-160	µA	VIN= GND RON=50kΩ
I_{PU}		-55	-165	-400	µA	VIN= GND RON=20kΩ
I_{PD}	Pull-down Current	22	66	160	µA	VIN= VDD RON=50kΩ
I_{PD}		55	165	400	µA	VIN= VDD RON=20kΩ

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Condition	Unit
V_{DD}	DC Supply Voltage	3.0 to 3.6	V
V_{IN} (5V Tolerant)	DC Input Voltage	-0.3 to 5.5	V
I_{OUT}	DC Output Current	± 30 (24mA Buffer)	mA
T_{STG}	Storage Temperature	-55 to 125 (Plastic)	°C

Table 4. Recommended Operating Conditions

Symbol	Parameter	Condition	Unit
V_{DD}	DC Supply Voltage	3.0 to 3.6	V
T_A	Commercial Temperature	0 to 70	°C

4.0 SmartMedia Timing

T_{cycle} : Min = 80 ns

4.1 AC Characteristics

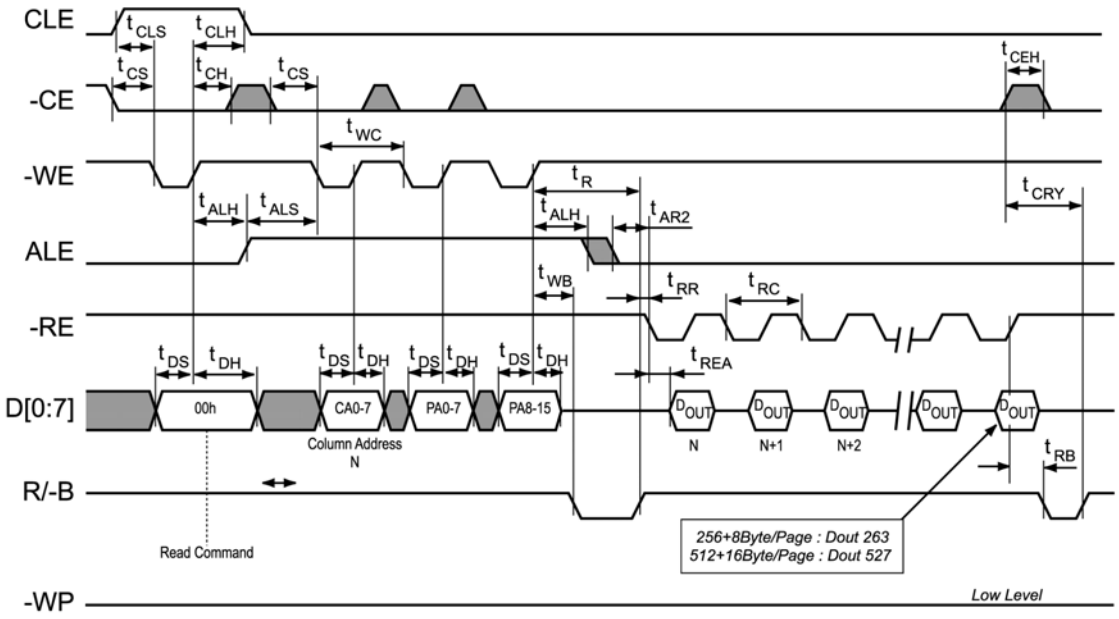
Table 5. SmartMedia AC characteristics

Symbol	Parameter	Min.		Max		Unit
		SM Spec	xSil 248	SM Spec	xSil 248	
t_{CLS}	CLE Setup Time	20	60	-		ns
t_{CLH}	CLE Hold Time	40	100	-		ns
t_{CS}	-CE Setup Time	20	60	-		ns
t_{CH}	-CE Hold Time	40	100	-		ns
t_{WP}	-WE Pulse Width	40	66	-		ns
t_{ALS}	ALE Setup Time	20	60	-		ns
t_{ALH}	ALE Hold Time	40	100	-		ns
t_{DS}	Data Setup Time	30	60	-		ns
t_{DH}	Data Hold Time (not on waveforms drawn)	20	30	-		ns
t_{WC}	Write Cycle Time (not on waveforms drawn)	80	100	-		ns
t_{WH}	-WE High Hold Time	20		-		ns
t_{WW}	-WP High to –WE Time	100	-	-		ns
t_{RR}	Ready to – RE Low	20	100	-		ns
t_{RP}	Read Pulse Width	60	66	-		ns
t_{RC}	Read Cycle Time	80	100	-		ns
t_{REA}	-RE Access Time (Serial Data Access)	-		45	60	ns
t_{CEH}	-CE high Hold Time (at the Last Serial Read)	250		-		ns
t_{REAID}	-RE Access Time (ID Read) (not on waveforms drawn)	-	-	90	-	ns
t_{RHZ}	-RE High to Output Hi-Z	5		30		ns
t_{CHZ}	-CE High to Output Hi-Z	-		30		ns
t_{REH}	-RE High Hold Time	20		-		ns
t_{IR}	Output Hi-Z to –RE Low	0		-		ns
t_{RSTO}	-RE Access Time (Status Read)	-		45		ns
t_{CSTO}	-CE Access Time (Status Read)	-		55		ns
t_{RHW}	-RE High to –WE Low	0		-		ns
t_{WHC}	-WE High to –CE Low	50		-		ns
t_{WHR}	-WE High to – RE Low	60		-		ns
t_{AR1}	ALE Low to – RE Low(Address Register Read, ID Read) (not on waveforms drawn)	200		-		ns
t_{CR}	-CE Low to -RE Low (Data Register Read, ID Read) (not on waveforms drawn)	200		-		ns
t_{WB}	-WE High to Busy	-		200		ns
t_{AR2}	ALE Low to –RE Low (Read Cycle)	150		-		ns
t_{RB}	Last –RE High to Busy(at Sequential Read)	-		200		ns
t_{CRY}	-CE High to Ready *	-		1		µs
t_R	Data Transfer Time (from Cell to Register)	-		100µs	8s	

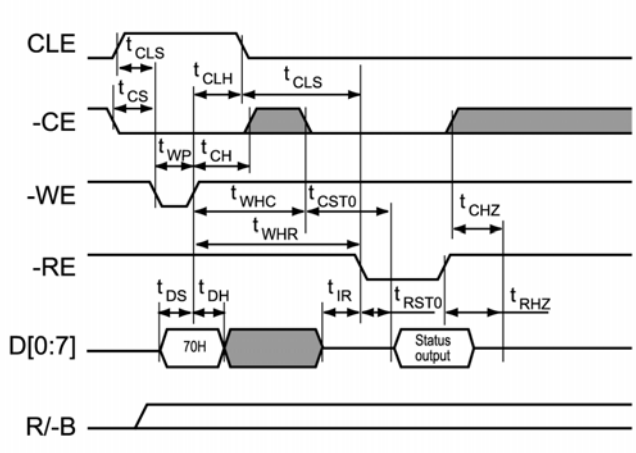
Symbol	Parameter	Min.		Max		Unit
		SM Spec	xSil 248	SM Spec	xSil 248	
t_{PROG}	Program Time	-		20ms	8s	
t_{BERAS}	Block Erase Time	-		400ms	8s	

* The length of the period between –CE High and Ready depends on the pull-up resistance at the Ready/-Busy terminal.

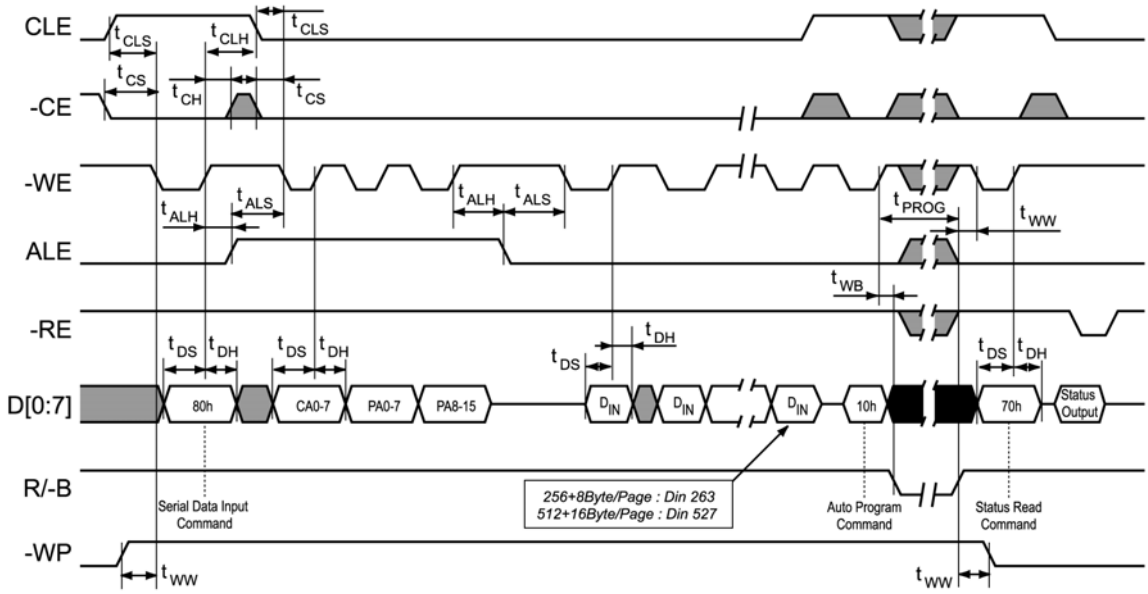
4.2.1 Read Cycle Timing Waveforms - 1MByte to 32MByte



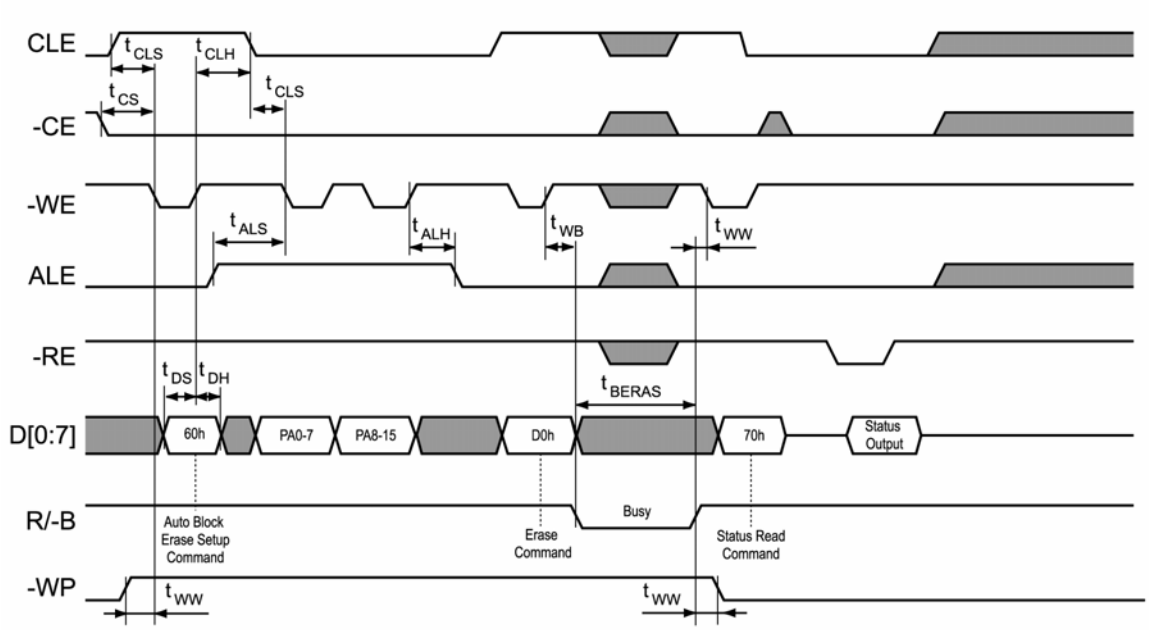
4.2.2 Status Read Timing Waveforms - 1MByte to 32MByte



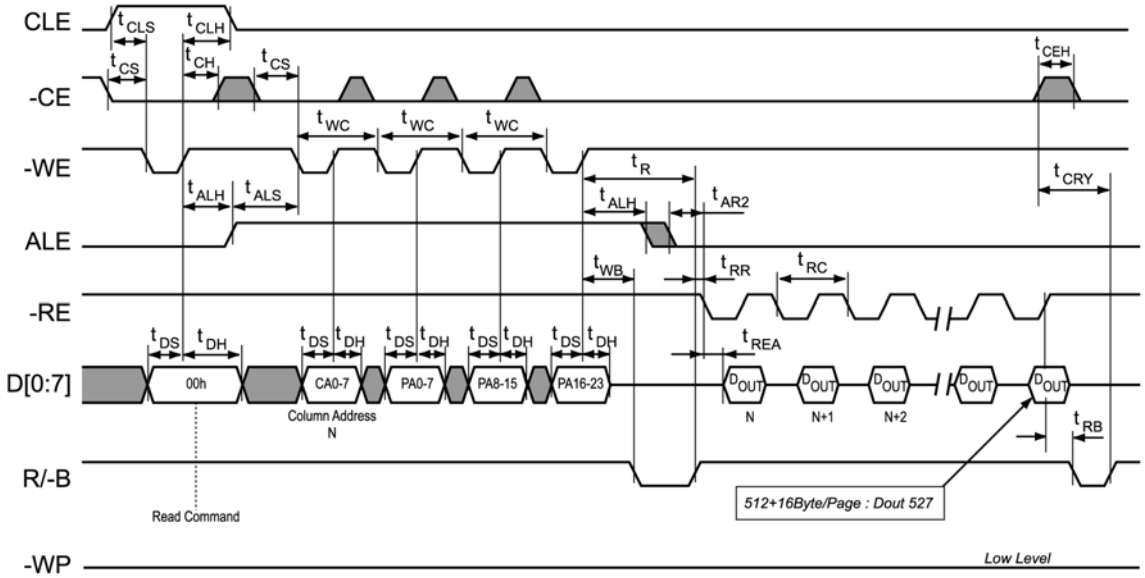
4.2.3. Autopage Timing Waveforms - 1MByte to 32MByte



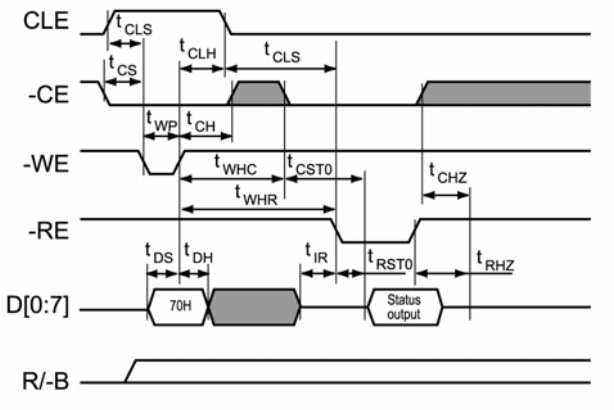
4.2.4 Auto Erase Timing Waveforms - 1MByte to 32MByte



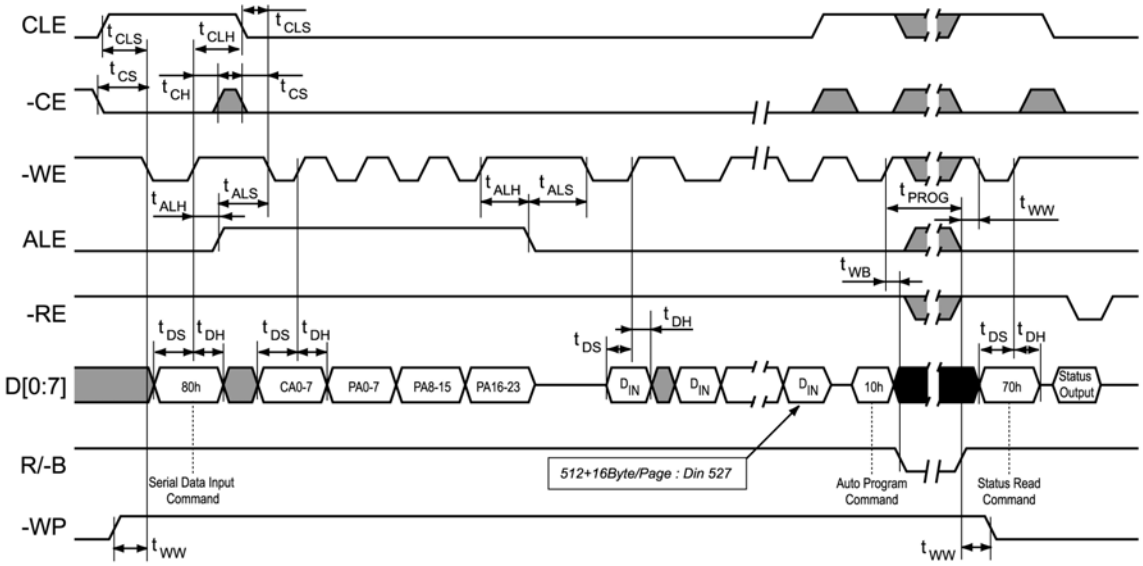
4.3.1 Read Cycle Timing Waveforms - 64MByte to 128MByte



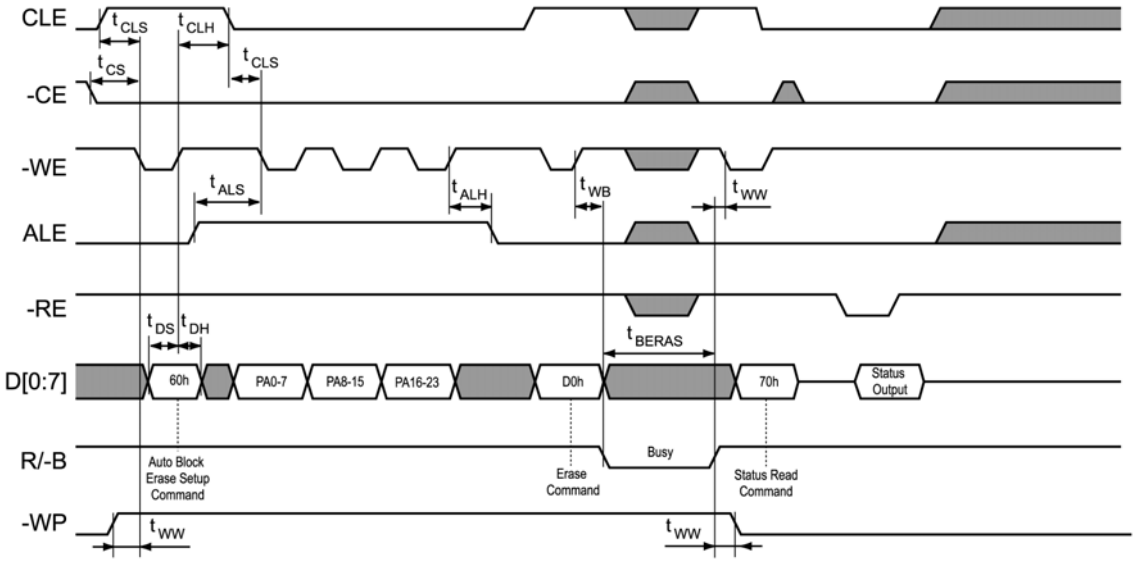
4.3.2 Status Read Timing Waveforms - 64MByte to 128MByte



4.3.3 Autopage Timing Waveforms - 64MByte to 128MByte



4.3.4 Auto Erase Timing Waveforms - 64MByte to 128MByte



5.0 xD Picture Card Timing diagrams

T_{cycle} : Min = 80 ns

5.1 AC Characteristics

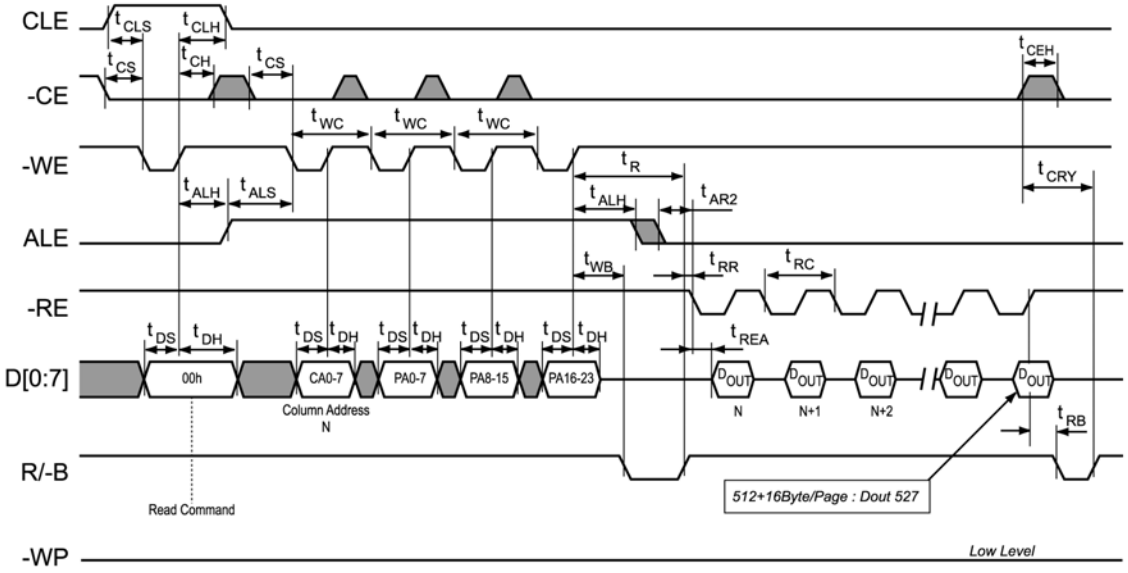
Table 6. xD Picture Card AC characteristics

Symbol	Parameter	Min.		Max		Unit
		xD Spec	248	xD Spec	248	
t_{CLS}	CLE Setup Time	20	60	-		ns
t_{CLH}	CLE Hold Time	40	100	-		ns
t_{CS}	-CE Setup Time	20	60	-		ns
t_{CH}	-CE Hold Time	40	100	-		ns
t_{WP}	-WE Pulse Width	40	66	-		ns
t_{ALS}	ALE Setup Time	20	60	-		ns
t_{ALH}	ALE Hold Time	40	100	-		ns
t_{DS}	Data Setup Time	30	60	-		ns
t_{DH}	Data Hold Time (not on waveforms drawn)	20	30	-		ns
t_{WC}	Write Cycle Time (not on waveforms drawn)	80	100	-		ns
t_{WH}	-WE High Hold Time	20		-		ns
t_{WW}	-WP High to –WE Time	100		-		ns
t_{RR}	Ready to – RE Low	20		-		ns
t_{RP}	Read Pulse Width	60	66	-		ns
t_{RC}	Read Cycle Time	80	100	-		ns
t_{REA}	-RE Access Time (Serial Data Access)	-		45	60	ns
t_{CEA}	-CE Access Time (Serial Data Access)	-		55		ns
t_{CEH}	-CE high Hold Time (at the Last Serial Read)	100		-		ns
t_{OH}	Output Data Hold Time	10		-		ns
t_{RHZ}	-RE High to Output Hi-Z	-		30		ns
t_{CHZ}	-CE High to Output Hi-Z	-		20		ns
t_{REH}	-RE High Hold Time	20		-		ns
t_{IR}	Output Hi-Z to –RE Low	0		-		ns
t_{RHW}	-RE High to –WE Low	0		-		ns
t_{WHR}	-WE High to – RE Low	50		-		ns
t_{AR1}	ALE Low to – RE Low(Address Register Read, ID Read) (not on waveforms drawn)	100		-		ns
t_{AR2}	ALE Low to –RE Low (Read Cycle)	50		-		ns
t_{CR}	-CE Low to -RE Low (Data Register Read, ID Read) (not on waveforms drawn)	100		-		ns
t_{WB}	-WE High to Busy	-		200		ns
t_{RB}	Last –RE High to Busy(at Sequential Read)	-		200		ns
t_{CRY}	-CE High to Ready *	-		6+tr(RY/-BY)		µs

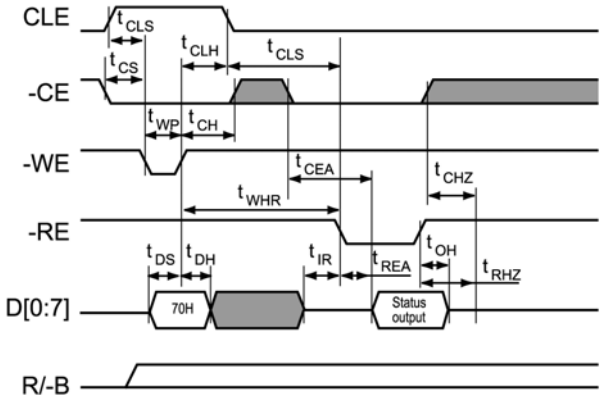
Symbol	Parameter	Min.		Max		Unit
		xD Spec	248	xD Spec	248	
t_R	Data Transfer Time (from Cell to Register)	-		6 2.9**	20	ms
t_{PROG}	Program Time	-		10	20	ms
t_{BERAS}	Block Erase Time	-		10	20	ms

* The length of the period between –CE High and Ready depends on the pull-up resistance at the Ready/-Busy terminal.
** Only for Read only device.
Note: Blank entries reflect no min or max value.

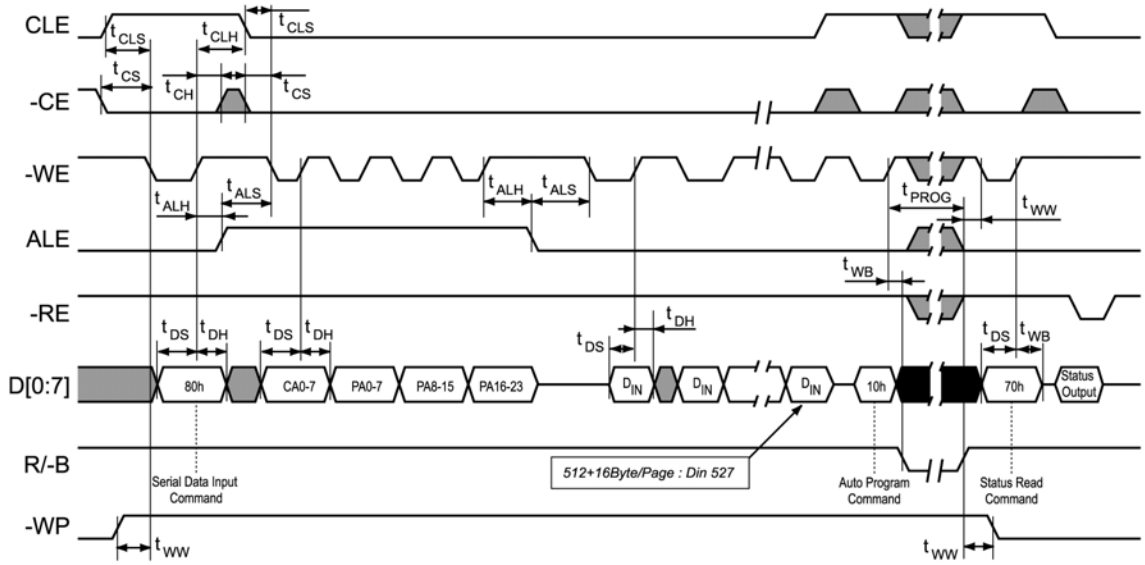
5.2 Read Cycle Timing Waveforms



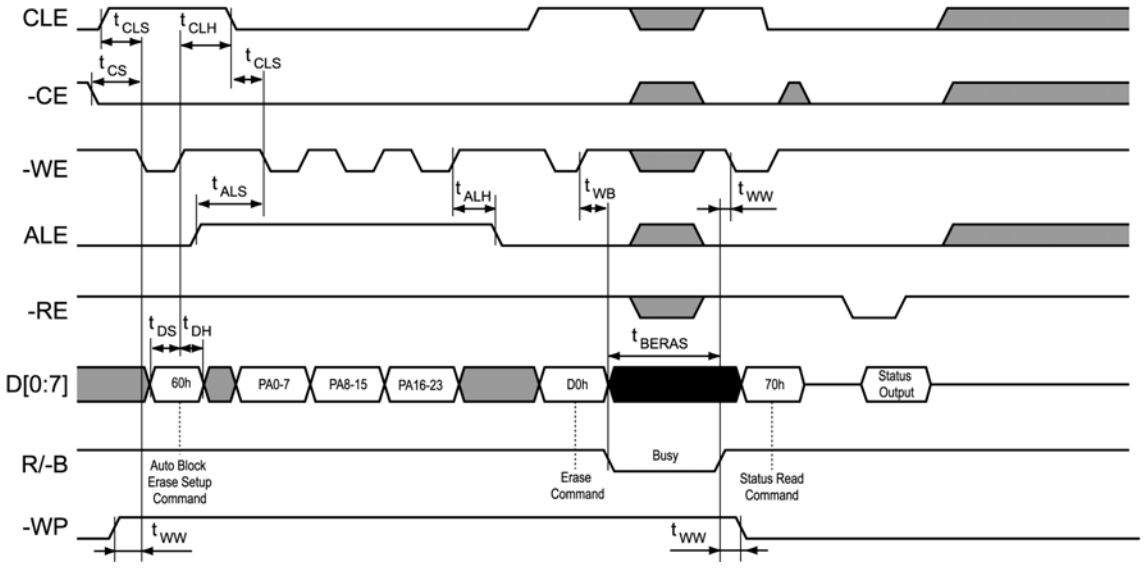
5.3 Status Read Timing Waveforms



5.4 Autopage Timing Waveforms



5.5 Auto Erase Timing Waveforms



6. CompactFlash Timing

xSil 248 accesses CompactFlash media in 16-bit Memory mapped mode. Upto PIO Mode 5 (20MB/sec Read and Write speeds) is supported.

7. Secure Digital Timing

Secure Digital Card and its electrical equivalents such as the miniSD, TransFlash, microSD and SD HS are accessed in 4-bit mode.

8. MultiMediaCard Timing

MultiMediaCard V1.x and V2.x compliant cards are accessed in 1-bit mode. MMC 3.x and 4.x cards are accessed in 4-bit mode. The timing for 4-bit mode is similar to the Secure Digital Card access.

9.Memory Stick Timing

Memory Stick Classic media are accessed in 1-bit mode. Memory Stick High Speed media and High Speed enabled Duo media are accessed in 4-bit mode. The timing is similar to the Memory Stick PRO accesses.

10. Memory Stick PRO Timing

11. MMC 4.0 Host Operation

11.1 Features

- Ideal for portable and stationary applications
- Host read-only, read/write and I/O cards
- Host operation supports 20MHz, 24MHz, and 48MHz clock frequencies
- Maximum data rate up to 384 Mbit / sec
- MMC support for 1bit (default), 4 bit and 8 bit
- Supports multiple command sets
- MultMediaCard Mode
    - Ten-wire bus (clock, 1 bit command, 8 bit data bus)
    - Card selection executes through an assigned unique card address for backward compatibility
    - One card per MMC bus.
    - Easy identification and assignment of session address
    - Error-protected data transfer
    - Sequential and Single/Multi block Read/Write commands

11.2 MMC Communication Signals

The xSil 248 MMC host transfers data via a configurable number of data bus signals.

11.2.1 MMC Card CLK Command

The xSil 248 host communicates with the MMC card's CLK signal allowing one bit transfer on each cycle of the CLK command and each one of the data lines is performed. The frequency may vary between zer and the maximum clock frequency.

11.2.2 MMC Card CMD Command

The xSil 248 MMC host communicates with the MMC card's CMD bidirectional command which is used for the MMC card initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the MMC Bus master to the card and responses are sent from the card to the host.

11.2.3 MMC Card DAT0-DAT7

The xSil 248 communicates with the MMC card's bidirectional data channels. The MMC's DAT signals operate in push-pull mode. The MMC includes interanl pull ups for all data lines. Only the card or the xSil 248 MMC host is driving these signals at a time. By default, after power up or reset, only the DAT0 channel is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the MMC controller.

11.2.4 MMC Card Classes

The xSil 248 supports the different MMC card classes
Read Only Memory (ROM) cards: The fixed data content is ideal for distribution media for software and consumer electronic applications.

Read/Write (RW) cards: RW type cards include Flash, One Time Programmable (OTP), and Multiple Time Programmable (MTP). These cards are typically sold as blank and used for mass storage, digital images, video recording, and audio applications.
I/O Cards: Typical applications for this card are communications as with modems. They will often have an additional interface link for outside communications.

11.3 MMC Card Interface Pin Connections

MMC Card Pins	Name	Description
1	DAT3	Data
2	CMD	Command/Response
3	V_{SS1}	Supply voltage ground
4	V_{DD}	Supply voltage
5	CLK	Clock
6	V_{SS2}	Supply voltage ground
7	DAT0	Data
8	DAT1	Data
9	DAT2	Data
10	DAT4	Data
11	DAT5	Data
12	DAT6	Data
13	DAT7	Data

11.4 MMC Card Registers

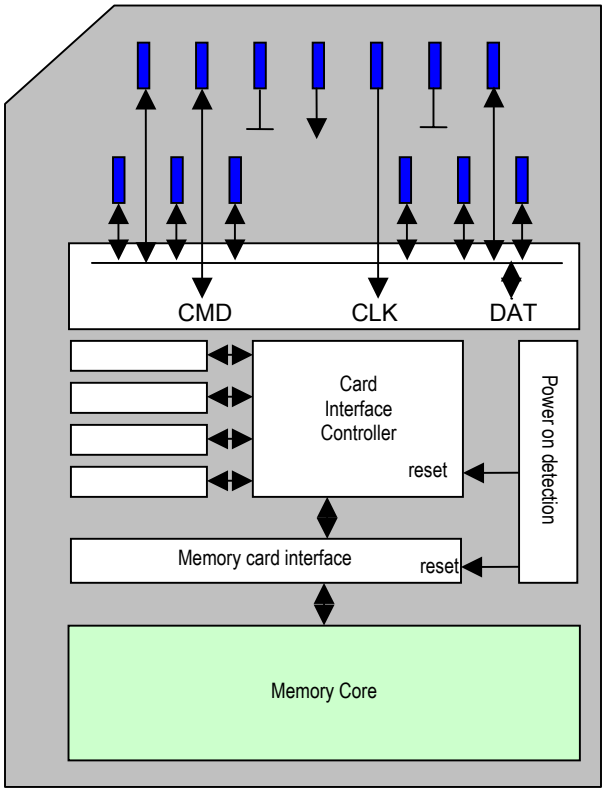
The xSil248 communicates with the MMC's initialization that uses only the CMD channel which is compatible with all of MMC classes. Each card has a set of information registers. The registers are defined below.

MMC Register Name	Width (bytes)	Description	Implementation
CID	16	Card IDentification number, a card individual number for identification.	Mandatory
RCA	2	Relative Card Address, is the card system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the card's output drivers.	Optional
CSD	16	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the card.	Mandatory
OCR	4	Operation Condition Register, Used by a special broadcast command to identify the voltage type of the card.	Mandatory
EXT_CSD	512	Extended Card Specific Data. Contains information about the card capabilities and selected modes. Introduced in specification V4.0	Mandatory

11.5 xSil 248 MMC Card Host Reset

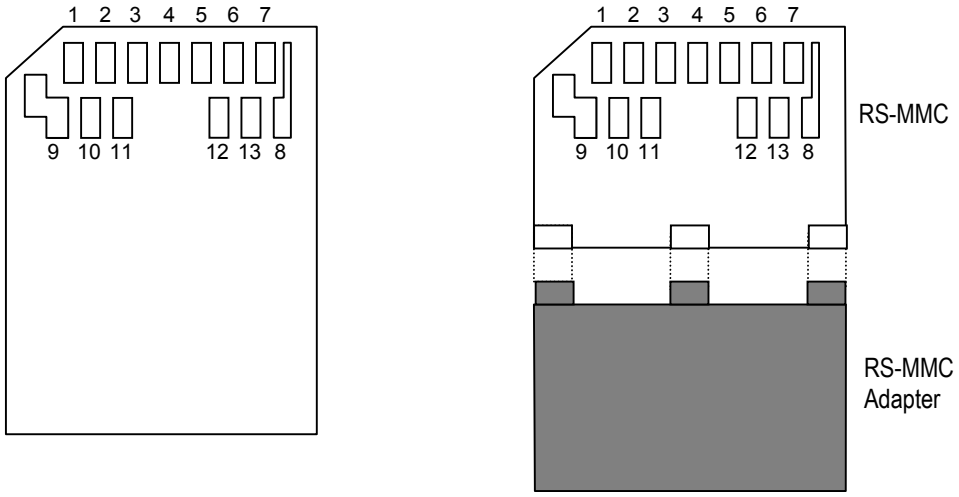
The xSil 248 MMC host may reset the card by switching the power supply off and back on. The MMC card should have its own power-on detection circuitry which puts the card into a defined state after the power-on. No explicit reset signal is necessary. The card can also be reset by it's own special command.

11.6 MMC Card Architecture



11.7 MMC Form Factor

The MMC has two form factors. The normal size form factor is 24mm x 32mm x 1.4mm. The reduced size form factor is 24mm x 18mm x 1.4mm. To use a reduced size MMC in a normal size MMC socket, a special adaptor has to be used. The figure below demonstrates the two form factors. The mechanical and electrical interface is identical in both form factors.



11.8 MMC Bus Concept

The xSil248 MMC bus is designed to connect either to solid-state mass-storage memory or I/O devices in a card format for multimedia applications. The xSil 248 MMC bus allows slow to fast data transfer rates satisfying the requirements for a wide range of applications. The xSil 248 operates as a single master bus with a single slave. The xSil 248's MMC bus master is the bus controller and the slave is either a single small storage MMC card or an I/O-card with its own controlling unit (on card) to perform the data transfer. The bus master includes power connections to supply the cards. The bus communication use a the MMC bus protocol. The payload data transfer between the host and the card can be bidirectional.

11.9 MMC Bus Lines

The xSil 248 MMC bus lines can be divided into three groups:

- Power supply: V_{SS1} and V_{SS2}, and V_{DD} are used to supply power to the cards.
- Data transfer: CMD, DAT0-DAT7 are used for bidirectional communications
- Clock: CLK is used to synchronize data transfer across the bus.

11.10 MMC Bus Protocol

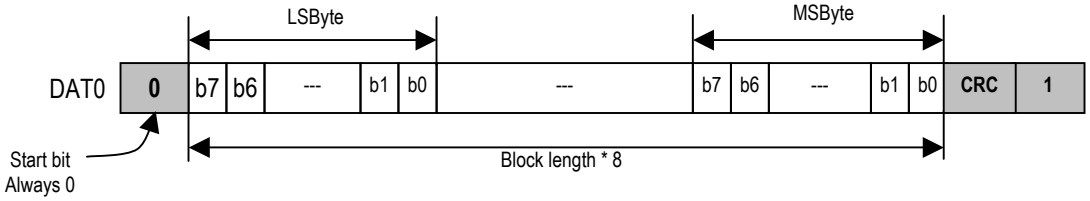
After a power-on reset, the xSil 248's MMC Host must initialize the card by a special message based MMC bus protocol. Each message is represented by one of the following tokens:

- Command: a command is a token, which starts an operation. A command is sent from the host to a card. A command is transferred serially on the CMD line.
- Response: a response is a token, which is sent from the card to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines. The number of data lines used for the data transfer can be 1(DAT0), 4(DAT0-DAT3) or 8(DAT0-DAT7).

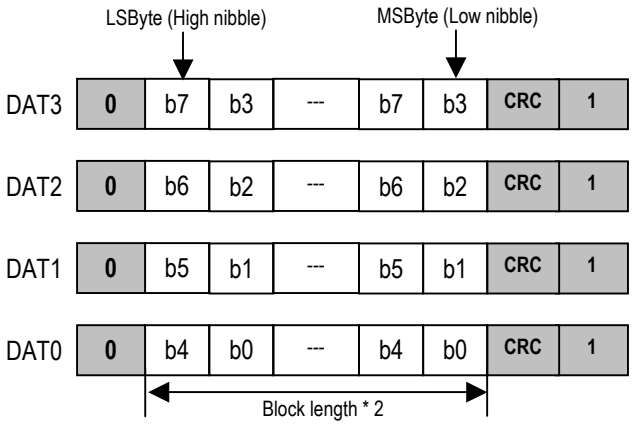
Card addressing is implemented using a session address, assigned during the initialization phase, by the bus controller to the connected card. Its CID number identifies a card. This method requires the card to have a unique CID number. To ensure uniqueness of CIDs the CID register contains 24 bits, which are defined by the MMCA. Every card manufacturer is required to apply for an unique MID (and optionally OID) number

Sequential Data

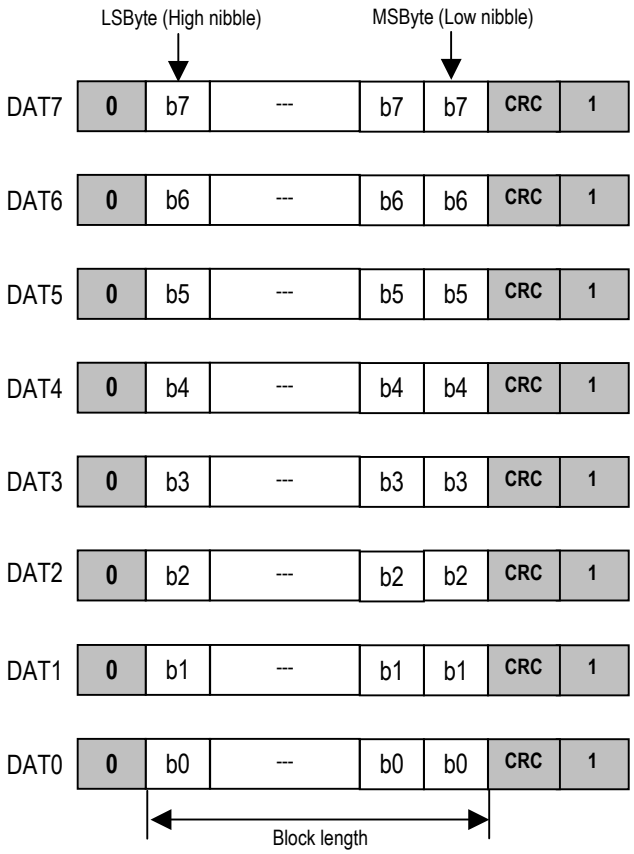
Block Data



4 Bits bus (DAT3-DAT0 used)

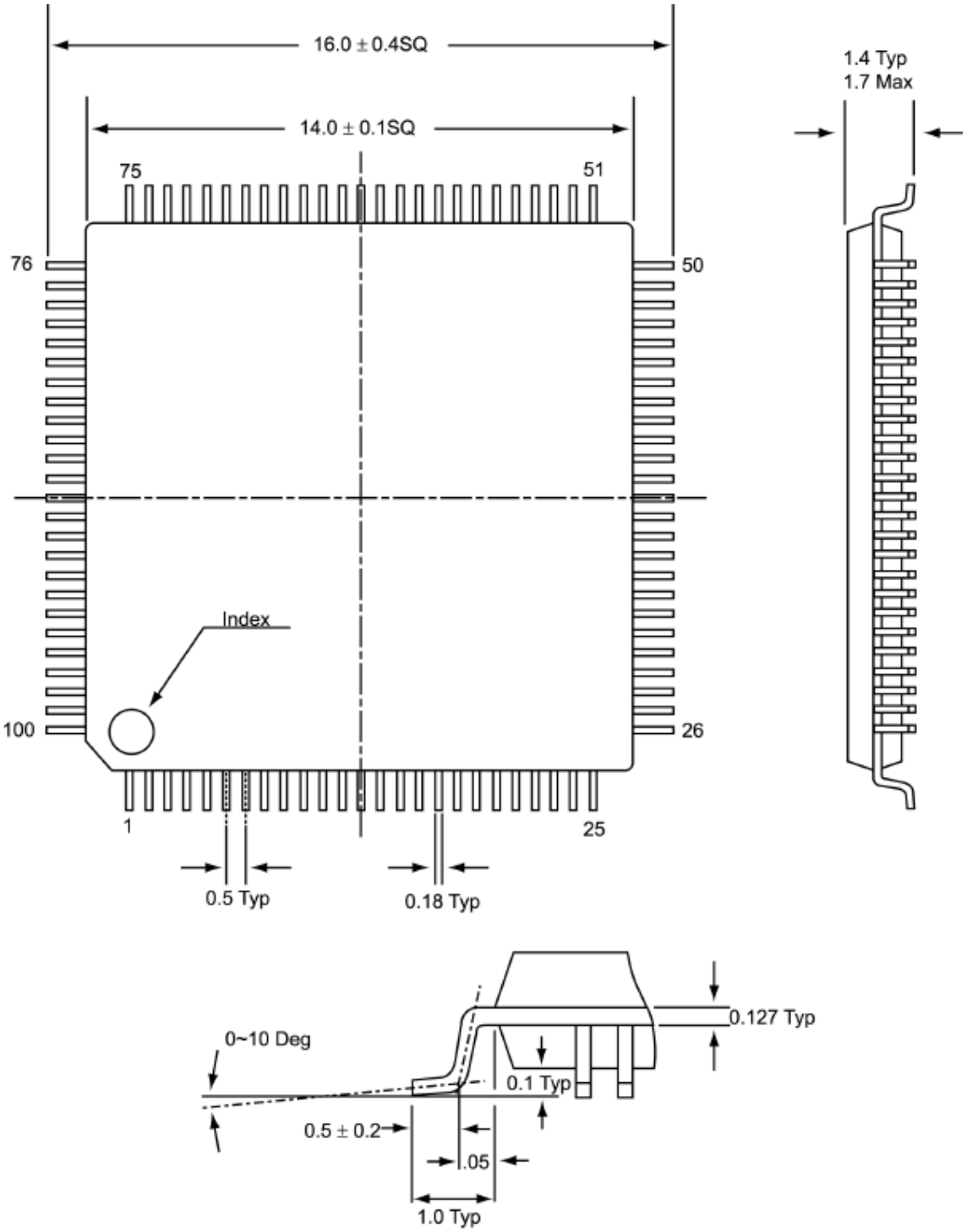


8 Bits bus (DAT7-DAT0 used)



12. Package Drawing

12.1.1 100-pin package



Note: Dimensions in mm

13. Part Number Ordering Information

Table 7. Part Number Ordering Information

Part Number	Description	Packaging
xSil 248	USB 2.0 CF I&II, Microdrive, SmartMedia, MS Duo, MS Pro Duo, MS, MS Pro, MMC, RS MMC, PCMCIA, xD, SD, NAND/MLC, Mini SD Read Write Controller	100 LQFP Leaded
xSil 248-G	USB 2.0 CF I&II, Microdrive, SmartMedia, MS Duo, MS Pro Duo, MS, MS Pro, MMC, RS MMC, PCMCIA, xD, SD, NAND/MLC, Mini SD Read Write Controller	100 LQFP Lead Free Green type package.